JSS Academy of Technical Education
Bengaluru

Invited Talk

Department of Electronics and Communication Engineering

Level: National

Title: Need for System Verilog, Verification Tools, Trends and opportunities in Industry.

Category: Invited talk

Date: 15th May 2021 (1 day)

No. of Resource Persons: 01

No. of Participants: 50 (6th Semester ECE Students)

Organizers: Department of Electronics and Communication Engineering

Resource Person(s) with Designation: Mr. Aditya Rangan
Senior Engineer
Open-Silicon Research Pvt. Ltd. (Sifive)

Mode: Online

Objective:

To create awareness about Need for SystemVerilog, Verfication Tools, Trends and opportunities in Industry.

Report: Brief report on the respective sessions held on Day-1 (15th May 2021, 9:00AM to 11:00AM)

Verification is the process of checking the correctness of design functionality. Functionality checking, Reusability, increasing the confidence/conviction, adding value to design are some of the factors which necessitates verification. Importance of verification and types of verification viz., front end and back end were discussed. Also, various verification methods such as Test Bench -- Scenarios and TestCases, Assertions Based and Functional and Code Coverage were explained in detail.

The verification flow was dealt in detail from specification to verification closure. System specifications, is nothing but technical representation of design intent. The design is given to the testbench plan and test plan where it determines the effort needed to validate the quality of the application under test and describes the test strategy, objectives, schedule, estimation, deliverables, and resources required to perform testing for a software product. The test bench readiness reads the testbench plan and the test case coding codes an input and an expected

output to verify a program's actual output against its expected output. Then the testbench readiness and test case code is passed to simulation, wherein if there is an error found, it is given back to the testbench readiness to fix the issue and test case coding to fix the issue with test cases. As the error is resolved the code is sent to the verification analysis to evaluate whether a product, service, or system complies with regulations, specifications, or conditions imposed at the start of a development phase. Verification gap is solved by the test plan and the new testbench features are done by the testbench plan. Later the verification analysis is given to the verification closure which achieves the closure to the question or problem at hand and makes it easier to move on to the next issue.

Also, the need for SystemVerilog, base for methodologies - UVM, VMM, OVM etc, tools used like -ncsim (Cadence), vcsim (Synopsys), EDA playground (Freeware) etc were briefed.

All students appreciated the talk and were enthralled to know concepts of SystemVerilog, Verification tools and the current trends and opportunities in Industry.

Outcome:

1. Exposure to the need for SystemVerilog, Verification Methodologies and Tools used for verification.
2. Introduction to the current Industry trends in Verification.

Annexure

Include brochure/Invitation

Certificate

JSS MAHAVIDYAPEETHA

JSS ACADEMY OF TECHNICAL

Department of Electronics

SEMINAR ON

Need for Verfication Trends and in

ALUMNI INITIATIVE-

Aditya Rangan
Senior Engineer
Open-Silicon Research Pvt.Ltd(Sifive)

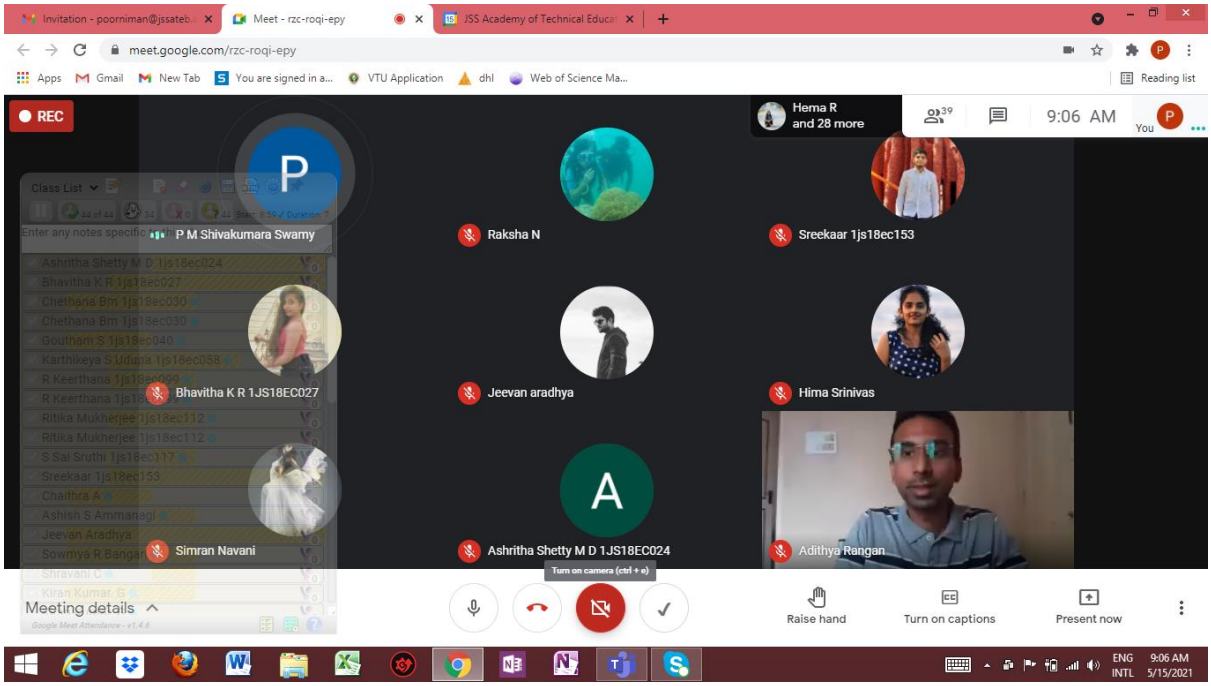
15-05-2021

09:00AM

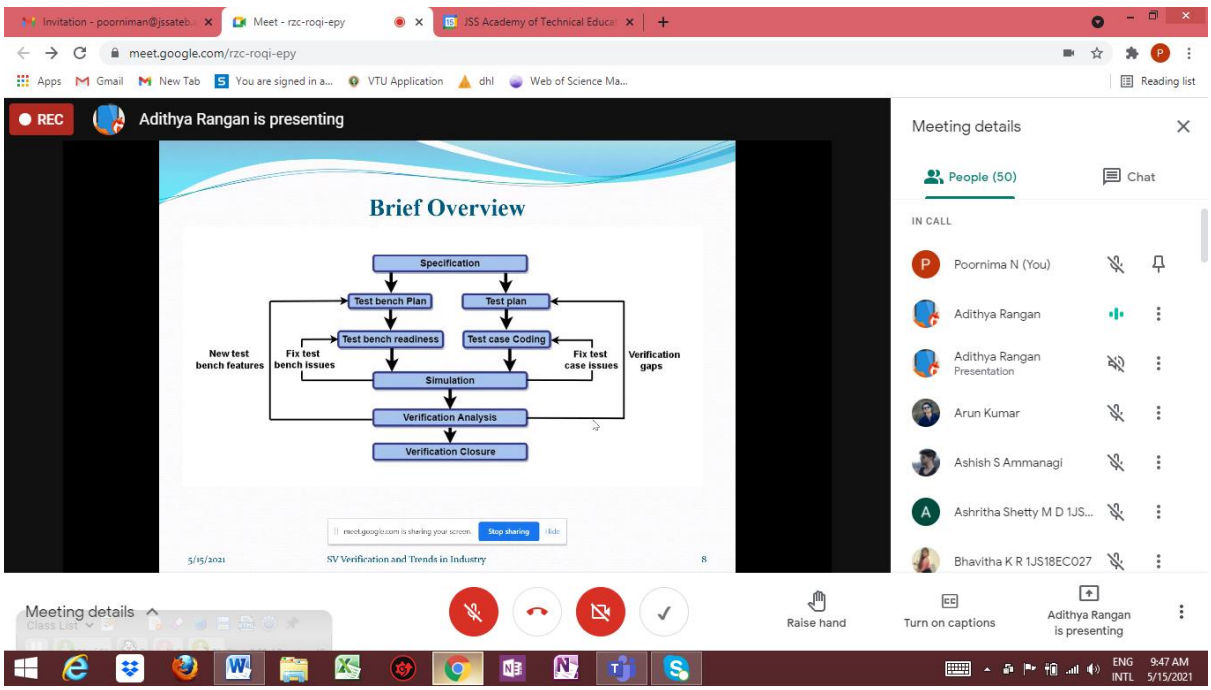
Nil

Photographs of session/s (with captions)

Mr. Aditya Rangan delivering invited talk to students in online mode.



Mr. Aditya Rangan, presenting contents on system verilog to students in online mode.



Brief Profile of the Resource person with their photograph.

Mr. Adithya Rangan completed his Master of Technology in VLSI Design and Embedded Systems from JSSATEB in 2016. Also, he was University Gold medalist. He was working as Design Verification Engineer at Innovative Logic Design Services Pvt. Ltd, Bangalore from 2016-2019. At present he is working as Senior Engineer at Open-Silicon Research Pvt. Ltd. (Sifive). His research interests include VLSI design and Verification and he has published eight research publications. Apart from technical skills, Aditya is aVedic Scholar and Preceptor with more than 2 decades of Vedic Chants Healing Technique.

Mr. Aditya Rangan C K

Senior Engineer I

Open-Silicon Research Pvt. Ltd. (Sifive), Bangalore.